(19) **Federal Republic of Germany**

German Patent Office

(12) **Patent Application Publication**
(11) **DE 3516989 A1**

(51) Int. Cl. [4]:
G 06F 1/00
H 05 K 7/20

[stamp:] Official property

(21) File Ref. No.: P 35 16 989.3
(22) Date of Application: May 10, 85
(43) Date of Disclosure: November 13, 86

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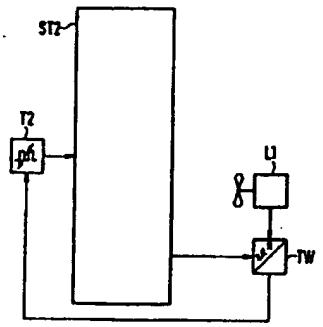
(54) Control unit with a device for removal of generated dissipation heat

In a control unit (ST2) with CMOS component groups, the timer frequency of an operating timer (T2) is switched, in case of a failure, to a value, for which the generated dissipated heat is uncritical with certainty, or the timer frequency is regulated to a lower value, for which the maximum permissible operating temperature is reached.



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Patent Claims

1. Control unit, in particular computer system, in which a number of CMOS component groups are operated in synchrony by means of the regulating pulse of a timer and whereby a device for removing the dissipated heat generated in the control unit, as well as a device for detection of too low removal of the dissipation heat and triggering of a corresponding failure signal are provided, characterized in that, as the timer, a timer (T2) with variable frequency is provided, and that, the operating timer frequency of the timer is reducible in case of a failure signal.

2. Control unit according to claim 1, characterized in that the timer frequency can be reduced continuously up to a certain value, at which the resetting of the failure signal is triggered.

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Control unit with a device for removal of the generated dissipation heat

The invention relates to a control unit, in particular a computer system, in which a number of CMOS component groups are operated in synchrony by the regulating pulse frequency of a timer and whereby a device for the removal of the dissipated heat generated in the control unit, as well as a device for detecting a too low heat dissipation and triggering of a corresponding control system are provided.

Large computer systems require in general cooling by means of cooling units, for example fans, so that a pre-specified maximum operating temperature is not exceeded. Redundant cooling systems are provided, if full operation of the computer system must be ensured in case of a failure of the cooling unit. However, if only the emergency operation of the computer system must be ensured in case of a total or a partial failure of the cooling unit, it is also possible, in computer systems with multiprocessor technology, that the individual processors are switched off and the important processes are divided among the remaining processors.

The underlying problem of the invention is to design a control unit of the kind mentioned at the outset, so that in case of malfunction of a cooling unit, an emergency operation is possible even in the case of monoprocessor systems.

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This problem is solved, according to the invention, in that, as the timer, a timer with a variable timer frequency is provided, and that, in case of a failure signal, the operating timer frequency of the timer can be reduced.

In the invention, use was made of the fact that in component groups with CMOS technology, the power consumption, and hence, the generated lost heat, is essentially dependent on the set timer frequency.

By means of this invention, during the emergency operation a markedly uniform distribution of heat is ensured, due to which, the heat removal during an emergency operation is positively influenced.

An advantageous enhancement of the invention is characterized in that the timer frequency can always be reduced continuously up to a certain value, on reaching which, a reset of the failure signal is triggered. In contrast to the reduction of the timer frequency to a fixed lower value, with which the operation can be guaranteed even without a cooling unit, in case of the regulation of the timer frequency, one always obtains the maximum possible timer frequency, and consequently the highest possible processing speed.

An exemplary embodiment of the invention is shown in the drawing and is explained in detail in the following. Shown are:

Fig. 1 An arrangement in principle of a control unit and the associated cooling unit and

Fig. 2 A block diagram of the invention.

In the view in Fig. 1, a control unit ST1, for example a computer system, is shown, which comprises the component groups B1 to B4, with which, for instance, one processor is associated. The operation of the control unit ST1 is

regulated by at least one timer T1. For the control unit ST1, a fan L1 is allocated, which removes the dissipated heat generated during the regular operation. Further, a temperature monitor TW is provided, which monitors the temperature of the control unit ST1 and/or the rate of rotation of the fan L1. In case of a failure, a corresponding failure signal is transmitted to the control unit ST1 by the temperature monitor TW, which leads, for example, to shutdown of the component groups B1 and B4 and the emergency operation is maintained by means of the component groups B2 and B3, shown together by the dashed line.

If the emergency operation of the control unit ST1 is not permissible, a redundant cooling unit, for example a fan L2, indicated by the dashed line line, is actuated to work.

The invention is represented by the block circuit diagram of the view according to Fig. 2. The elements that are the same as in Fig. 1 are represented by identical reference symbols.

The invention assumes, as the prerequisite, as mentioned at the outset, that an emergency operation with reduced computer power should be allowed. Therefore, a redundant cooling unit is not provided. Further, it is assumed that as the control unit, a control unit ST2 with CMOS component groups is provided, in which the generated dissipation heat depends on the timer frequency of the system.

From the temperature monitor TW, in case of an outage of the fan L1 and/or impermissibly high temperature in the control unit ST2, a failure signal is transmitted to the timer T2, which has, in contrast to the timer T1 (Fig. 1), a

variable timer frequency. In case of a failure, the timer frequency is either switched to a value that is uncritical even in the case of a complete outage of the cooling unit, whereby this value lies above the minimum timer frequency of the used CMOS component groups, or the timer frequency of the timer is reduced only to such an extent that the permissible operating temperature of the control unit ST2 is not exceeded. While in the first case only a switching over of the timer T2 between two timer frequencies (upper and lower timer frequency) takes place, in the second case, the regulation of the timer frequency to values between the upper and the lower timer frequency is necessary. Despite the increased circuitry for that, the maximum processing speed of the control unit ST2 is always ensured.

~~2 Patent Claims~~
~~2 Figures~~

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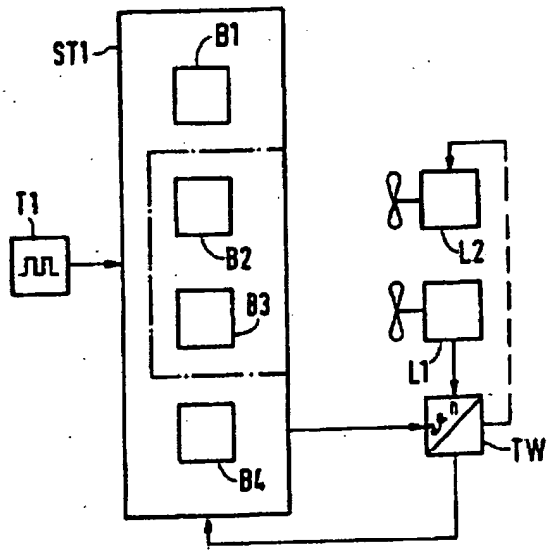

FIG 1

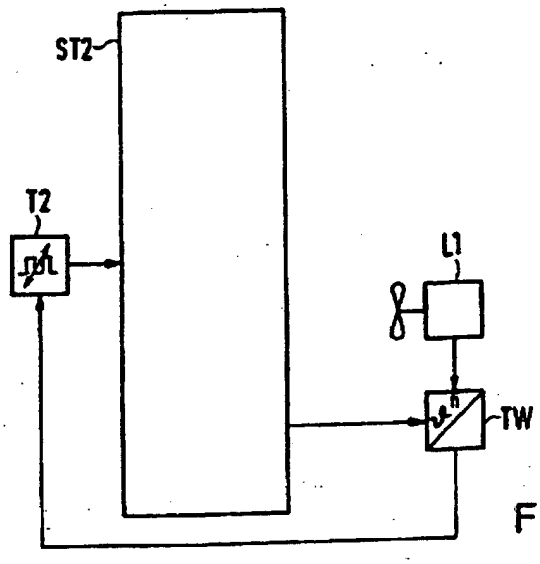

FIG 2